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IEC 61508 SOFT ERRORS RATE (SER) REVIEW

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Introduction

This paper provides a review of the effects of 'Soft Errors' in relation to IEC 61508[1] random hardware failures assessments.

General

IEC 61508:2010 requires the assessment of random hardware failures (whether it's Probability of Failure on Demand - PFD or Probability of Dangerous Failure per Hour - PFH) to include the failure rate for the devices incorrectly functioning due to software error caused by the temporary change in the stored program in the memory module. This paper examines the reality of this type of temporary error leading to an actual malfunction of the device.

Source of soft errors

The dominant source of soft errors is to high energy cosmic rays caused by Neutron particles, which create a charge when arriving at the substrate. At 10,000 ft there are about 10 times more neutrons than at sea level.

Potential effects on types of memory

Over the last ten years, manufacturers have improved Dynamic Random Access Memory (DRAM) considerably; in particular; the packaging. Also the planar capacitor cells, previously used to store the signal charge, have been changed to 3D capacitor designs that significantly increase the critical charge that would be needed to affect the cell state. This now makes most DRAM devices more hardened against all types of soft error. As chip volumes per bit have also reduced, the amount of charge collected from an event has also decreased helping even further. The result is that over time the Soft Error Rate (SER) per bit of DRAM has reduced over 1000 times

If an older system using 1Mbit of DRAM had the DRAM chip replaced with one of today's hardened devices, the SER would reduce by over 1000 times

Static Random Access Memory (SRAM) is a little different. Over time, the junction capacitance and voltage has reduced as the technology has got smaller. The smaller technology collects a smaller amount of charge from an SER event however; the beneficial effect is negated by the smaller junction capacitance and smaller voltage. This means that the SER per BIT is similar to that of older devices.

Soft error detection

Memory manufacturers usually design the device layout so that a multi bit upset will not affect many bits within the same word, allowing the change to be detected by parity or ECC detection.

If the bit is an I/O state, the effect will only be present until the data is updated

One of the most common mechanisms to detect a soft error is by the use of parity or by error detection and correction (ECC)

The drive to miniaturize, increase speed, reduce cost and increase design flexibility has meant that many hardware design components are implemented using Field Programmable Gate Arrays (FPGAs) and similar devices.

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[1] IEC 61508:2010. Functional Safety of Electrical/Electronic/Programmable Electronic Safety-related Systems

There are now FPGA devices available with soft error detection units (SEDU) built in

Manufacturers Memory Test Data

Manufacturer's data for FPGAs and SRAM are typically around 700 FIT / 1 Mbit. However, SDRAM manufacturers have done much to harden them, so for a particular manufacturer we see values from 5 FIT / 1 Mbit for a180nm Fab Process, down to .007 FIT / 1 Mbit for a 68nm device (measured in accordance with JEDEC methods JESD889A). Even adding a correction factor to increase the confidence level above the 60% stated by the manufacturer brings this well below the FPGA and SRAM number stated above (4 or 5 orders better in some instances).

Detection of soft memory errors

In many cases, if this soft errors, the hardware diagnostics may pick up the changes.

For new designs many FPGA vendors have added soft error detection units (SEDU) to the device itself so the device configuration tools add the appropriate parity to internal memory so that an SER error can be detected

Hardware measures can be put in place to detect soft errors during initial design and so remove the effect; however, such measures would be difficult to apply to existing hardware.

Software measures can be applied to help detect soft errors and hence could be applied to existing systems if needed.

Recorded actual field soft failure rates

Although the published test result for soft error rates indicated by some memory manufacturers give a higher failure rate than the equivalent memory hardware failure rate, one logic controller manufacturer has included software diagnostic in their systems to trap and record these types of soft failures. To date the number of soft error failures recorded are significantly less than the hardware failure rate.

There appears to be a significant lack of collected data on soft failures in actual working operational devices. Where product manufacturers have tried to collect this data the indications are that the actual failure rates are significantly less than the memory hardware failure rate, therefore when considering a complete sub-system there is no significant increase to the hardware failure rates.